REMARKS

In this Amendment, Applicants have amended claims 1 and 6 to correct a typographical error and to improve grammar. Claims 1-9 remain pending.

In the Office Action, the Examiner rejected claims 1 and 6 under 35 U.S.C. § 102(e) as anticipated by Park et al. (U.S. Patent No. 6,648,508); rejected claims 1 and 6 under 35 U.S.C. § 102(b) as anticipated by Ohno (U.S. Patent No. 5,801,443); rejected claims 1 and 6 under 35 U.S.C. § 102(e) as anticipated by Chern et al. (U.S. Publication No. 2002/0098699); rejected claims 1-6 and 9 under 35 U.S.C. § 103(a) as unpatentable over Park et al. or Ohno or Chern et al. in view of Cooper et al. (U.S. Patent No. 5,219,793); and rejected claims 7-8 under 35 U.S.C. § 103(a) as unpatentable over Park et al. or Ohno or Chern et al. further in view of Chang et al. (U.S. Patent No. 6,159,842) and further in view of Tsai et al. (U.S. Patent No. 6,331,480). Applicants note that the detailed discussion of the Office Action indicates that the Examiner also rejected claim 3 under 35 U.S.C. § 102(e) as anticipated by Park et al., Office Action, p. 3; rejected claims 3 and 4 under 35 U.S.C. § 102(b) as anticipated by Ohno, Office Action, p. 4; rejected claim 3 under 35 U.S.C. § 102(e) as anticipated by Chern et al., Office Action, p. 5. Applicants respectfully traverse these rejections.

Regarding the rejections under 35 U.S.C. § 102, Applicants submit that none of the applied references teach each and every element of the rejected claims. The Examiner is respectfully reminded that, in order to properly anticipate Applicants' claimed invention under 35 U.S.C. §102, each and every element of the claim in issue must be found, "either expressly or inherently described, in a single prior art reference."

"The identical invention must be shown in as complete detail as is contained in the . . . claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." *See* M.P.E.P. § 2131, 8th ed., 2001.

Independent claim 1 recites a method for forming contact openings that includes, "a) forming bit line patterns on a substrate; b) forming an interlayer insulating layer over the substrate; c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns; and d) forming spacers on sidewalls of the bit line patterns only exposed through the contact opening." None of Park et al., Ohno, and Chern et al. teaches each and every element of claim 1.

First, Park et al. is directed to methods of forming integrated circuit devices using self-aligned contact hole fabrication steps. Particularly, "[r]eferring to FIG. 5A, a photoresist pattern 27 is formed. . . . Next, the exposed upper interlayer insulating layer 26 and the capping insulating layer 24 are dry-etched . . . , thereby forming a relatively narrow and deep contact hole, (e.g., a first contact hole 32) exposing a first portion of the first pad plug 10a." Park et al., col. 5, ll. 36-44. "[R]eferring to FIG. 5C, . . . the upper interlayer insulating layer 26 and the capping layer 24 are dry-etched . . . using the mask pattern 28 and the mask spacer 30 as etching masks." Id., col. 6, ll. 8-31. "Referring to FIG. 7, the protrusion 24a of the capping insulating layer 24 is dry-etched to expose . . . of pad plugs 10a and 10b."

The Examiner considered Park et al.'s bit line patterns 22 as corresponding to Applicants' claimed bit line patterns and capping insulating layer 24 and upper interlayer

insulating layer 26 as corresponding to Applicants' claimed interlayer insulating layer. Office Action, p. 3. However, Park et al. clearly fails to teach etching insulating layers 24 and 26 using bit line patterns 22 as a mask. In other words, Park et al. fails to teach at least "etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask," as recited in claim 1.

Moreover, Fig. 1 of Park et al. shows that pad plug 10a is approximately in a shape of a square. Consequently, Park et al.'s "narrow and deep contact hole" 32 cannot be a "straight line shaped self-aligned contact opening," as recited in claim 1. In other words, Park et al. also fails to teach at least "forming at least one straight line shaped self-aligned contact opening," as recited in claim 1.

The Examiner also considered Park et al.'s spacer 34 as corresponding to Applicants' claimed spacers. Office Action, p. 3. However, Park et al. teaches that "an oxide spacer 34 . . . is formed on a sidewall of the second contact hole 32a" (Id., col. 6, ll. 63-65, and Fig. 6), rather than on sidewalls of bit line patterns 22, allegedly corresponding to Applicants' claimed bit line patterns. Therefore, Park et al. fails to teach at least "forming spacers on sidewalls of the bit line patterns only exposed through the contact opening," as recited in claim 1.

In summary, Park et al. fails to teach at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns; and d) forming spacers on sidewalls of the bit line patterns only exposed through the contact opening," as recited in claim 1.

Second, Ohno is directed to a method of forming a contact hole for connecting a semiconductor substrate to a wiring layer or electrode. Ohno, col. 1, ll. 7-10. Relevant parts of Ohno relied on by the Examiner teach that "a photoresist is coated on the silicon dioxide film 14, and the resist pattern 16 having an opening portion 15 is formed by a photolithography process. . . . Using an etching process, the silicon dioxide film 14 is dry-etched by RIE techniques, and a contact hole 17a is formed." Id., col. 8, ll. 7-14, and FIG. 12. The Examiner considered Ohno's resist pattern 16 as corresponding to Applicants' claimed etching mask. Office Action, p. 4. However, Ohno fails to teach that resist pattern 16 defines a straight line shape. Neither does Ohno teach that contact hole 17a is "straight line shaped." In other words, Ohno fails to teach at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns," as recited in claim 1.

Finally, Chern et al. is directed to a method of forming a bit line and a node contact hole using a self-aligned contact etching process. Particularly, "[a]s shown in FIG. 7, . . . [a] photoresist layer 60 is [ ] formed . . . and a photolithographic process is performed to define the patterns of a node contact hole 61. As shown in FIG. 8, portions of both the dielectric layer 58 and the dielectric layer 50 are removed, following the [patterning of] the photoresist layer 60. Using the passivation layer 56 as a hard mask, a self-aligned etching process is performed to form the node contact hole 61." Chern et al., paragraph [0018] on p. 2. The Examiner considered Chern et al.'s patterned photoresist layer 60 as corresponding to Applicants' claimed etching mask.

Office Action, p. 4. However, Applicants note that Chern et al. fails to teach that photoresist pattern 60 defines a straight line shape. Neither does Chern et al. teach that node contact hole 61 is "straight line shaped." In other words, Chern et al. fails to teach at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns," as recited in claim 1.

Moreover, the Examiner considered Chern et al.'s spacers 50a as corresponding to Applicants' claimed spacers. However, according to Chern et al., "[t]he [ ] SAC etching process stops on the surface of the passivation layer 56, and the remaining dielectric layer 50 forms a spacer 50a . . . on the sidewall of the bit line 54a." Chern et al., paragraph [0020] on p. 2. Therefore, even assuming, *arguendo*, that Chern et al.'s node contact hole 61 corresponds to Applicants' claimed contact opening, Chern et al.'s spacers 50a are not formed on sidewalls of bit line 54a and passivation layer 56, allegedly corresponding to Applicants' claimed bit line patterns (Office Action, p. 4), **exposed through** node contact hole 61. Rather, spacers 50a are formed on sidewalls of bit line 54a, which is **NOT** exposed through node contact hole 61. In addition, only passivation layer 56 is exposed through node contact hole 61, while passivation layer 56 does **NOT** have a spacer formed thereon. Therefore, Chern et al. also fails to teach at least "forming spacers on sidewalls of the bit line patterns only exposed through the contact opening," as recited claim 1.

In summary, Chern et al. fails to teach at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as

a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns; and d) forming spacers on sidewalls of the bit line patterns only exposed through the contact opening," as recited in claim 1.

Thus, because none of Park et al., Ohno, and Chern et al. teaches each and every element of claim 1, claim 1 is allowable over these references under 35 U.S.C. § 102. Claims 3 and 4 depend from claim 1 and are also allowable under 35 U.S.C. § 102 at least because of their dependence from a allowable base claim.

Regarding the rejections under 35 U.S.C. § 103(a), Applicants first note that, as discussed above, all of Park et al., Ohno, and Chern et al. fail to teach or suggest at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns," as recited in claim 1.

Regarding the rejection of claims 1-6 and 9 under 35 U.S.C. § 103(a) as unpatentable over Park et al. or Ohno or Chern et al. in view of Cooper et al., Applicants submit that Cooper et al. fails to teach or suggest at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns," as recited in claim 1. See Amendment Under 37 C.F.R. § 1.116 filed on July 23, 2004, page 7. Therefore, Cooper et al. fails to overcome the deficiencies of Park et al., Ohno, and Chern et al., and claim 1 is allowable under 35 U.S.C. § 103(a) in view of these references. Claims 2-6 and 9

depend from claim 1 and are also allowable under 35 U.S.C. § 103(a) at least because of their dependence from an allowable base claim.

Regarding the rejection of claims 7-8 under 35 U.S.C. § 103(a) as unpatentable over Park et al. or Ohno or Chern et al. further in view of Chang et al. and further in view of Tsai et al., Applicants note that neither Chang et al. nor Tsai et al. cures the deficiencies of Park et al., Ohno, or Chern et al. with regard to claim 1. Chang et al. is directed to a method for fabricating a hybrid low dielectric constant intermetal dielectric layer (ABSTRACT of Chang et al.) and Tsai et al. is directed to a method for improving the adhesion between an overlying insulator layer and an underlying low K layer (ABSTRACT of Tsai et al.). Thus, Chang et al. and Tsai et al., taken alone or in combination, fail to teach or suggest at least "c) etching the interlayer insulating layer by using the bit line patterns and an etching mask defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns," as recited in claim 1. Therefore, claims 7-8, which depend from claim 1, are allowable under 35 U.S.C. § 103(a).

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of pending claims 1-9.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 4, 2005

By: _____
Qingyu Yin*

* With limited recognition under 37 C.F.R. § 10.9(b).